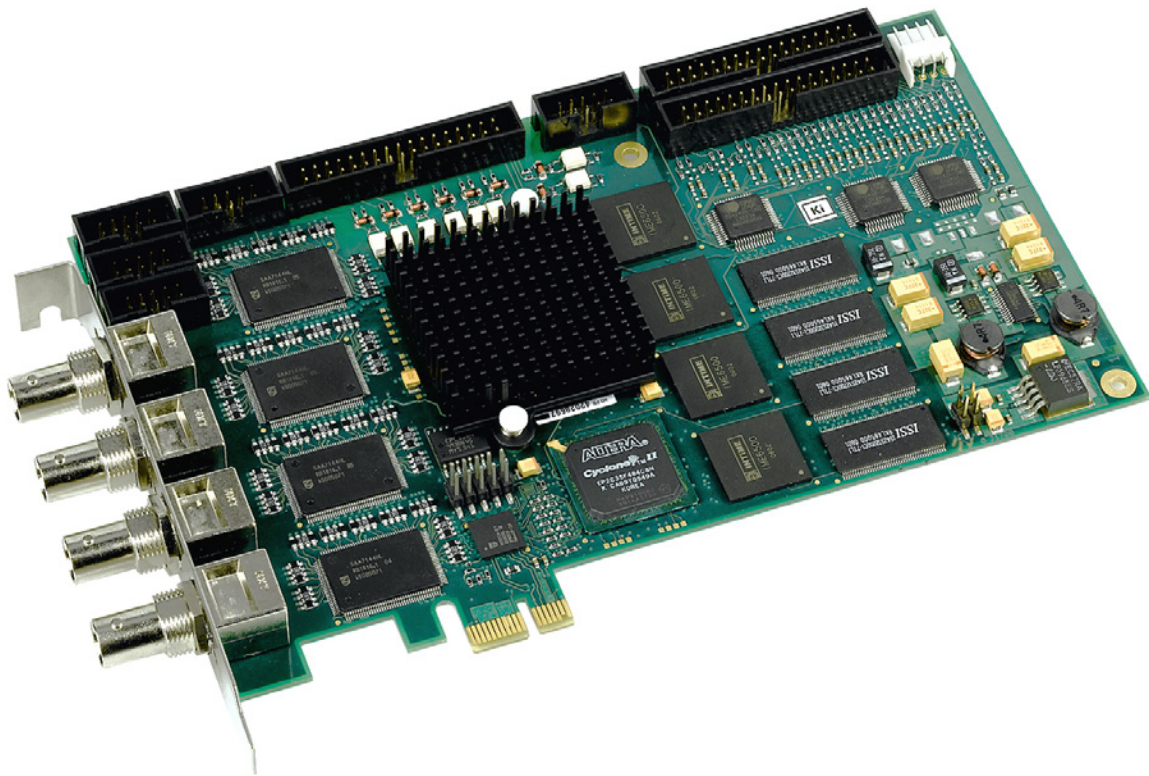


ELTEC

systems

# PC\_EYE/JPG

16-Channel PCI Express Frame Grabber for Security Applications



## HARDWARE MANUAL

Revision 0A



## Revision

Revision	Changes	Date / Name
oA	First Edition	14.11.06 pp

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### Federal communications commission statement

- This device complies with FCC Rules Part 15. Operation is subject to the following two conditions:
- This device may not cause harmful interference, and
- This device must accept any interference received including interference that may cause undesired operation.
- This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try correct the interference by one or more of the following measures:
  - Reorient or relocate the receiving antenna.
  - Increase the separation between the equipment and receiver.
  - Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
  - Consult the dealer or an experienced radio/TV technician for help.
- The use of shielded cables for connection of the monitor to the graphics card is required to assure compliance with FCC regulations. Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

### Canadian department of communications statement

- This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.
- This class B digital apparatus complies with Canadian ICES-003

## SAFETY INFORMATION

### Electrical safety

- To prevent electrical shock hazard, disconnect the power cable from the electrical outlet before reloading the system.
- When adding or removing devices to or from the system, ensure that the power cables for the devices are unplugged before the signal cables are connected. If possible, disconnect all power cables from the existing system before you add device.
- Before connecting or removing signals cables from motherboard, ensure that all power cables are unplugged.

- Make sure that your power supply is set to the correct voltage in your area. If you are not sure about the voltage of the electrical outlet you are using, contact your local power company.
- If the power supply is broken, do not try to fix it by yourself. Contact a qualified service technician or your retailer.

#### Operation safety

- Before installing the motherboard and adding devices on it, carefully read the manuals that came with the package.
- Before using the product, make sure all cables are correctly connected and the power cables are not damaged. If you detect any damage, contact your dealer immediately.
- To avoid short circuits, keep paper clips, screws, and staples away from connectors, slots sockets and circuitry.
- Avoid dust, humidity, and temperature extremes. Do not place the product in any area where it may become wet.
- Place the product on a stable surface.
- If you encounter technical problems with the product, contact a qualified service technician or your retailer.

#### EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

#### IMPOTANT INFORMATION

This product is not an end user product. It was developed and manufactured for further processing by trained personnel.

#### RECYCLING



Please recycle packaging environmentally friendly:

Packaging materials are recyclable. Please do not dispose packaging into domestic waste but recycle it.



Please recycle old or redundant devices environmentally friendly:

Old devices contain valuable recyclable materials that should be reutilized. Therefore please dispose .... old devices at collection points which are suitable.

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## HARDWARE MANUAL PC\_EYE/JPG

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### 1. Introduction

#### 1.1. About this Document

The purpose of this documentation is to describe the ELTEC Elektronik AG PC\_EYE/JPG frame grabber family. It contains a description of the hardware installation. The software package is common to all members of the frame grabber family.

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## HARDWARE MANUAL PC\_EYE/JPG

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## 2. Getting Started

### 2.1. Requirements

What you need for installation and use of the PC\_EYE/JPG family member boards:

- The frame grabber board.
- Camera with CCIR/EIA analogue CVBS video output
- Camera Cable
- Computer system with free PCI Express X1 slot.
- Windows XP or a Linux operating system.
- Operating system dependent hardware driver setup and system independent development files (the driver can be downloaded from the website [www.eltec.de](http://www.eltec.de)).

### 2.2. Hardware Installation

- Switch off computer.
- Prepare site to observe electrostatic discharge (ESD) precautions before opening computer or removing the grabber from its case: Touch computer steel case during insertion/removal of the frame grabber or take other precautions to ensure the absence of high voltages due to electric charges.
- Open computer case, remove blind back panel.
- Insert the board and the connector panel(s) into a free PCI Express slot; the board must fit into the slot without use of excessive force, make sure it sits firmly in the slot and the PCI Express connector conductors sit completely inside the connector.
- Fix the back panel with screw.
- Close case.

### 2.3. Connecting the Camera

Attach camera cable to camera connector no 1 as shown by the arrow in the picture below.

#### 2.3.1. Frontpanel

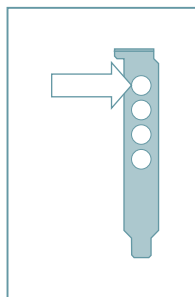


Figure 1: Frontpanel

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## HARDWARE MANUAL PC\_EYE/JPG

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### 3. Hardware Reference

#### 3.1. Introduction

This manual describes 4 different boards. If you are not sure which kind of board you have, see the label at the largest IC on the topside of the frame grabber.

##### 3.1.1. General Features

- Frame grabber for 16 simultaneous non-synchronized (free-running) CVBS cameras
- Real-time acquisition of images or image sequences directly into main memory
- Image memory formats include YCrCb (4:1:1, 4:2:2 and 4:4:4), RGB or BGR with 24 and 32 bits / pixel and Monochrome with 8 bits/pixel
- 4 or 16 channel input with individual ADCs (SAA7113)
- Scaling 1:2, 1:4 and 1:8 by pixel and line dropping
- JPEG encoder for each camera
- Programmable region of interest for each channel separately
- DMA target can be main memory or graphics memory
- One timer for Interrupt with 1.29 us granularity and 16 bit length
- 8 Opto-isolated output controls
- 8 Opto-isolated input controls
- PCI Express interface, 1 Lane width

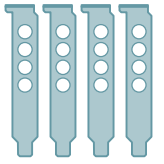
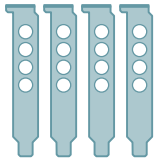


Note that you can use several boards -also of different type- in one computer, in this case the Board-IDs of the boards must be set to different values.

Not all frame grabber boards provide all features, for more details, see the table below:

**HARDWARE MANUAL PC\_EYE/JPG**

3.1.2. Differences between V-PCEY-710, V-PCEY-720, V-PCEY-730 and V-PCEY-740

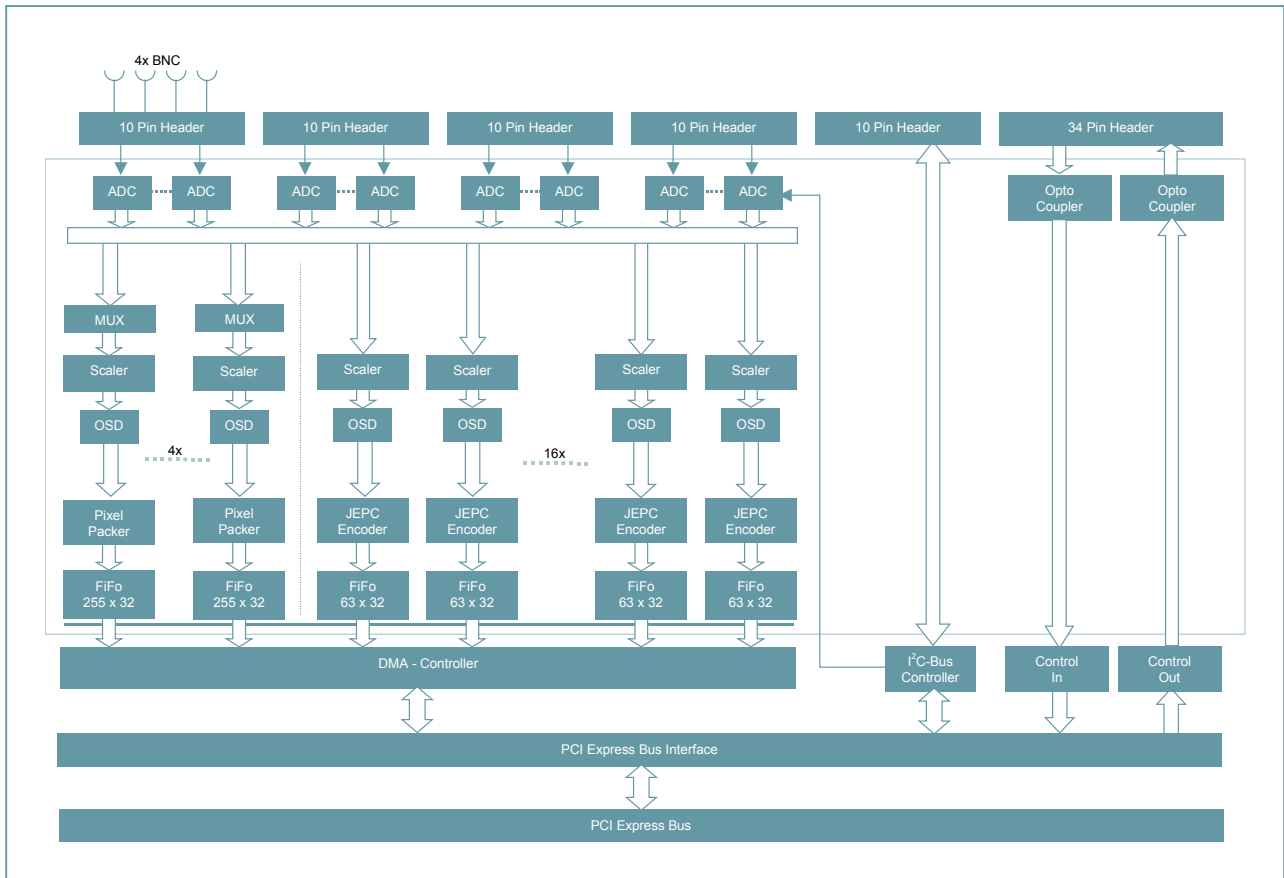
**Table 3.1: Differences between V-PCEY-710, V-PCEY-720, V-PCEY-730 and V-PCEY-740**

	V-PCEY-710	V-PCEY-720	V-PCEY-730	V-PCEY-740
CVBS Inputs	16	16	4	4
Simultaneous Uncompressed / JPEG Channels	4/16	4/-	4/4	4/-
Connectors	16 x BNC	16 x BNC	4 x BNC	4 x BNC
				

**HARDWARE MANUAL PC\_EYE/JPG**

3.2. V-PCEY-710 Hardware

3.2.1. Blockdiagram



**Figure 2: Blockdiagram V-PCEY-710**

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## HARDWARE MANUAL PC\_EYE/JPG

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### 3.2.2. Technical Details

The PC\_EYE/JPEG is intended for security applications, where video images from up to 16 monochrome or color cameras is acquired into a PC's main memory for storage, or the graphics board for display. Images are transferred by up to 20 DMA controllers. Four channels are dedicated for uncompressed processing and the other 16 channels are for JPEG compression. An on-board scaling unit can transform the full-resolution images to CIF size for smaller efficient display in split screen applications. Image format can be selected to be luminance / chrominance-separated (YUV) for optimum video detection or to be RGB for display.

### 3.2.3. Camera Signals

The frame grabber board interfaces to standard composite video (CVBS) color cameras, conforming to PAL (NTSC / SECAM) standards. The signals of the first four cameras are routed to the BNC connectors at the slot bracket. All camera signals are routed to the four on-board header-connector with 10 pins, intended for connection to separate I/O panels, each with four BNC.

### 3.2.4. ADC

There are 16 analog-to-digital converters (ADC) where up to 16 cameras can be connected to. Each camera has its own ADC (SAA 7113) as well as its own color separator. This makes it possible to switch cameras in the digital domain, minimizing multiplex times: Since the analog input is not switched, there is no PLL settling delay, which can take up to several frame times in other multiplexing schemes. The clock used for acquisition (13.5 MHz) is generated in the ADC chip. It is phase-locked to the horizontal sync.

### 3.2.5. Multiplexer

For the uncompressed data path, the digital input multiplexer assigns each of the four (DMA-) channels to one of the 16 ADC. It is possible to assign on ADC to multiple channels. For the JPEG compression path, all 16 ADC are connected directly to the 16 (DMA-) channels.

### 3.2.6. Scaler

The FPGA-based scaler can be used to reduce video data by line / pixeldropping over original pixels in blocks of 1x1, 2x2, 4x4, or 8x8. By using two DMA channels for storing the same video stream, simultaneous storage of scaled and non-scaled data is possible.

## HARDWARE MANUAL PC\_EYE/JPG

### 3.2.7. Uncompressed Channels

#### 3.2.7.1. Pixel Packer

To support different cameras and applications, there are several modes of storing pixel data in memory:

**Table 3.2: Pixel Packing Modes**

Mode Name	Description
Mono8	One monochrome image, byte-aligned
Y:U:V	YUV/YCbCr components are stored in 4:4:4, 4:2:2, or 4:1:1 mode
RGB	RGB24 uses 24 bits for each RGB pixel, RGB32 use 32-bit words with one zero-filled byte.

#### 3.2.7.2. FIFO

A FIFO associated with every DMA channel provides buffer space of 1 Kbytes to ensure uninterrupted acquisition even in situations with high PCI bus loads.

### 3.2.8. Compressed Channels

#### 3.2.8.1. JPEG Encoder

The JPEG encoder can encode all 16 color video streams in real-time. JPEG has been chosen as the coding scheme, since normal PC\_EYE/JPEG applications use multiplexed camera data, where interframe coding, such as MPEG, is not useful. Each field is stored in a separate JPEG file.

#### 3.2.8.2. FIFO

A FIFO associated with every DMA channel provides buffer space of 256 bytes to ensure uninterrupted acquisition even in situations with high PCI bus loads.

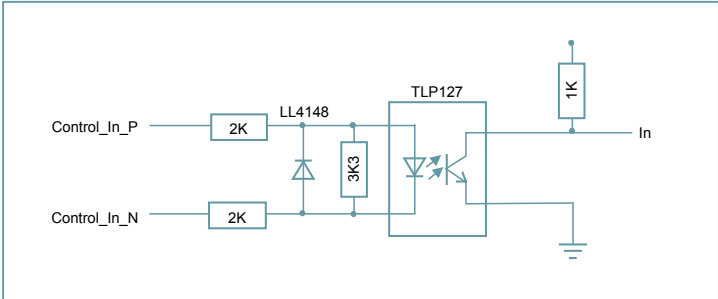
### 3.2.9. DMA Controller

In the last step, image data is transmitted by DMA directly into main memory. This DMA controller consists actually of 20 independent controllers, capable of transferring the video data stream into memory.

**HARDWARE MANUAL PC\_EYE/JPG**

**3.2.10. Opto-Isolated Input Controls**

For control purpose, there are 8 opto-isolated inputs. The inputs do not control any hardware flow, but can be read by software. The diagram below shows the opto-coupler connections:

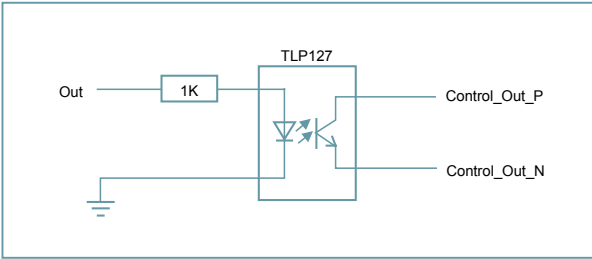


**Figure 3: Optocoupler Input**

An active state is detected, when the input voltage is 3 V or higher. The maximal Voltage is 30 V. For higher voltage, an additional resistor is needed.

**3.2.11. Opto-Isolated Output Controls**

For control purpose, there are 8 opto-isolated outputs. The outputs can be set by writing a register. The diagram below shows the opto-coupler connections:



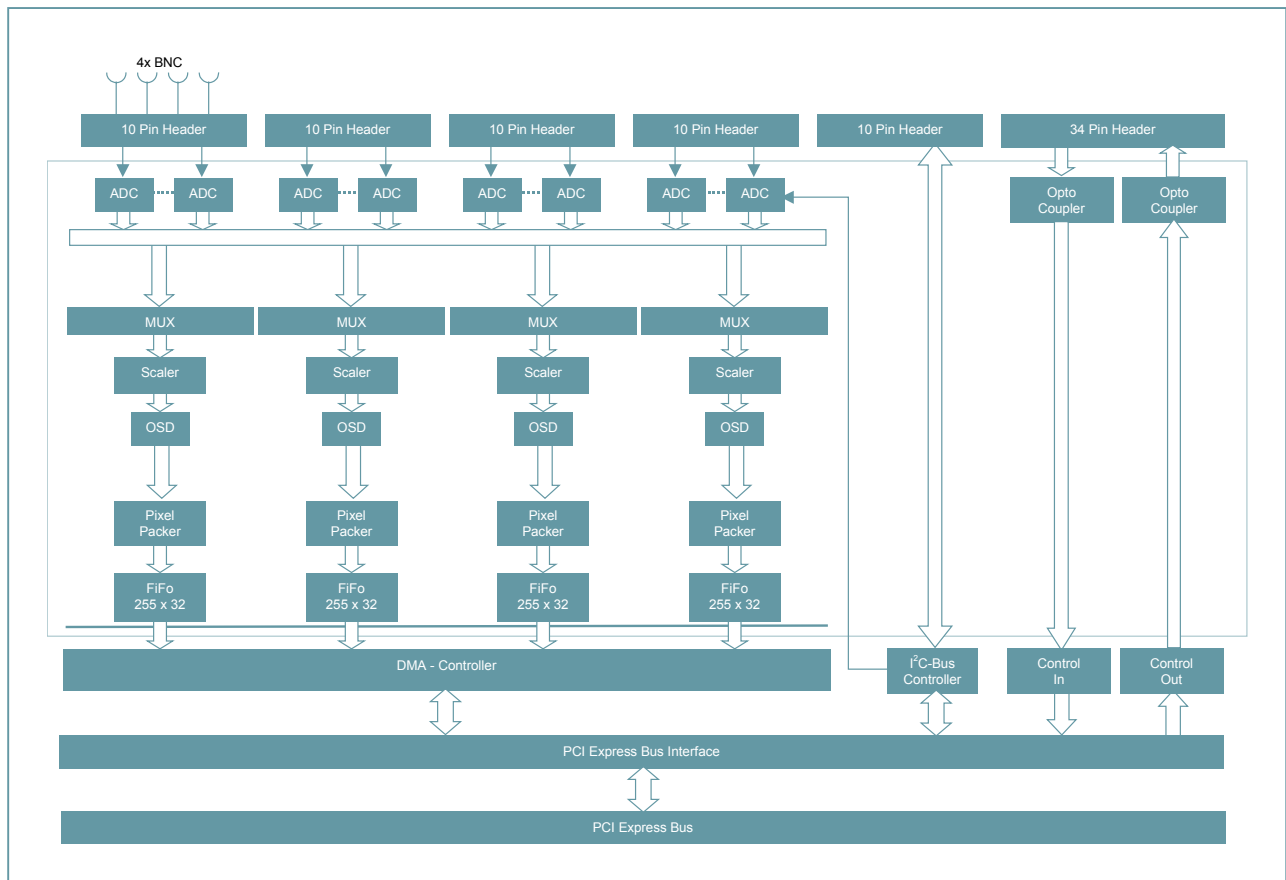
**Figure 4: Optocoupler Output**

The maximal allowed ON Current is 100 mA. The maximal allowed OFF Voltage is 50 V.

**HARDWARE MANUAL PC\_EYE/JPG**

3.3. V-PCEY-720 Hardware

3.3.1. Blockdiagram



**Figure 5: Blockdiagram V-PCEY-720**

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## HARDWARE MANUAL PC\_EYE/JPG

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### 3.3.2. Technical Details

The PC\_EYE/JPEG is intended for security applications, where video images from up to 16 monochrome or color cameras is acquired into a PC's main memory for storage, or the graphics board for display. Images are transferred by up to 4 DMA controllers. An on-board scaling unit can transform the full-resolution images to CIF size for smaller efficient display in split screen applications. Image format can be selected to be luminance / chrominance-separated (YUV) for optimum video detection or to be RGB for display.

### 3.3.3. Camera Signals

The frame grabber board interfaces to standard composite video (CVBS) color cameras, conforming to PAL (NTSC / SECAM) standards. The signals of the first four cameras are routed to the BNC connectors at the slot bracket. All camera signals are routed to the four on-board header-connector with 10 pins, intended for connection to separate I/O panels, each with four BNC.

### 3.3.4. ADC

There are 16 analog-to-digital converters (ADC) where up to 16 cameras can be connected to. Each camera has its own ADC (SAA 7113) as well as its own color separator. This makes it possible to switch cameras in the digital domain, minimizing multiplex times: Since the analog input is not switched, there is no PLL settling delay, which can take up to several frame times in other multiplexing schemes. The clock used for acquisition (13.5 MHz) is generated in the ADC chip. It is phase-locked to the horizontal sync.

### 3.3.5. Multiplexer

The digital input multiplexer assigns each of the four (DMA-) channels to one of the 16 ADC. It is possible to assign on ADC to multiple channels.

### 3.3.6. Scaler

The FPGA-based scaler can be used to reduce video data by line / pixeldropping over original pixels in blocks of 1x1, 2x2, 4x4, or 8x8. By using two DMA channels for storing the same video stream, simultaneous storage of scaled and non-scaled data is possible.

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## HARDWARE MANUAL PC\_EYE/JPG

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### 3.3.7. Pixel Packer

To support different cameras and applications, there are several modes of storing pixel data in memory:

**Table 3.3: Pixel Packing Modes**

Mode Name	Description
Mono8	One monochrome image, byte-aligned
Y:U:V	YUV/YCbCr components are stored in 4:4:4, 4:2:2, or 4:1:1 mode
RGB	RGB24 uses 24 bits for each RGB pixel, RGB32 use 32-bit words with one zero-filled byte.

### 3.3.8. FIFO

A FIFO associated with every DMA channel provides buffer space of 1 Kbytes to ensure uninterrupted acquisition even in situations with high PCI bus loads.

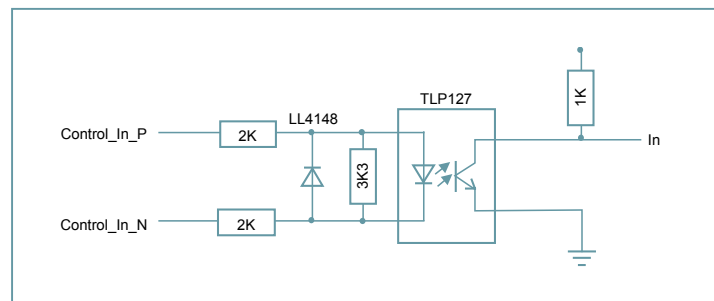
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## HARDWARE MANUAL PC\_EYE/JPG

### 3.3.10. Opto-Isolated Input Controls

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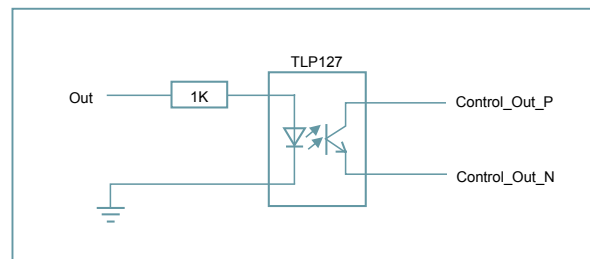


**Figure 6: Optocoupler Input**

An active state is detected, when the input voltage is 3 V or higher. The maximal Voltage is 30 V. For higher voltage, an additional resistor is needed.

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For control purpose, there are 8 opto-isolated outputs. The outputs can be set by writing a register. The diagram below shows the opto-coupler connections:



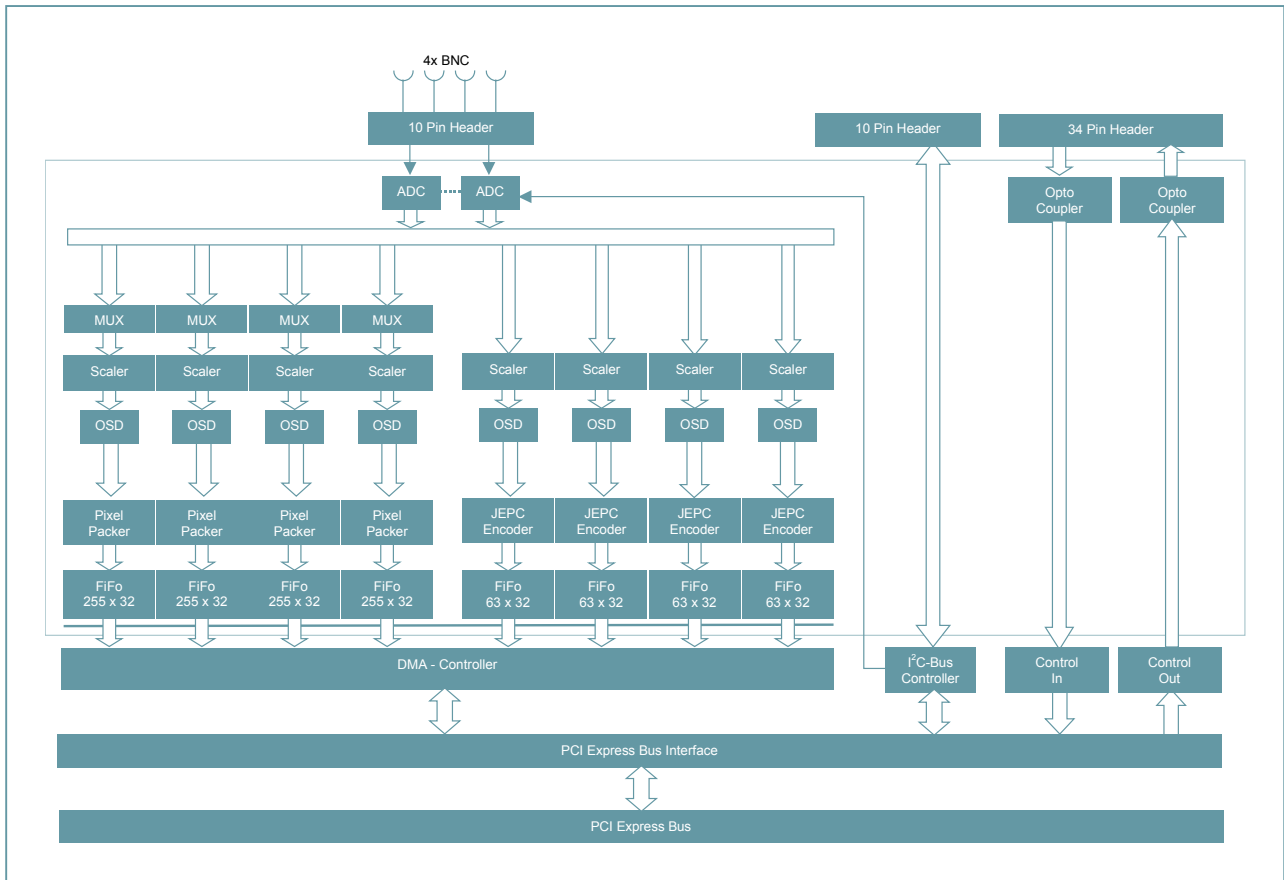
**Figure 7: Optocoupler Output**

The maximal allowed ON Current is 100 mA. The maximal allowed OFF Voltage is 50 V.

**HARDWARE MANUAL PC\_EYE/JPG**

3.4. V-PCEY-730 Hardware

3.4.1. Blockdiagram



**Figure 8: Blockdiagram V-PCEY-730**

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## HARDWARE MANUAL PC\_EYE/JPG

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### 3.4.2. Technical Details

The PC\_EYE/JPEG is intended for security applications, where video images from up to four monochrome or color cameras is acquired into a PC's main memory for storage, or the graphics board for display. Images are transferred by up to 8 DMA controllers. Four channels are dedicated for uncompressed processing and the other four channels are for JPEG compression. An on-board scaling unit can transform the full-resolution images to CIF size for smaller efficient display in split screen applications. Image format can be selected to be luminance / chrominance-separated (YUV) for optimum video detection or to be RGB for display.

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### 3.4.5. Multiplexer

For the uncompressed data path, the digital input multiplexer assigns each of the four (DMA-) channels to one of the four ADC. It is possible to assign one ADC to multiple channels. For the JPEG compression path, all four ADC are connected directly to the four (DMA-) channels.

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The FPGA-based scaler can be used to reduce video data by line / pixeldropping over original pixels in blocks of 1x1, 2x2, 4x4, or 8x8. By using two DMA channels for storing the same video stream, simultaneous storage of scaled and non-scaled data is possible.

## HARDWARE MANUAL PC\_EYE/JPG

### 3.4.7. Uncompressed Channels

#### 3.4.7.1. Pixel Packer

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RGB	RGB24 uses 24 bits for each RGB pixel, RGB32 use 32-bit words with one zero-filled byte.

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A FIFO associated with every DMA channel provides buffer space of 1 Kbytes to ensure uninterrupted acquisition even in situations with high PCI bus loads.

### 3.4.8. Compressed Channels

#### 3.4.8.1. JPEG Encoder

The JPEG encoder can encode all four color video streams in real-time. JPEG has been chosen as the coding scheme, since normal PC\_EYE/JPEG applications use multiplexed camera data, where interframe coding, such as MPEG, is not useful.

Each field is stored in a separate JPEG file.

#### 3.4.8.2. FIFO

A FIFO associated with every DMA channel provides buffer space of 256 bytes to ensure uninterrupted acquisition even in situations with high PCI bus loads.

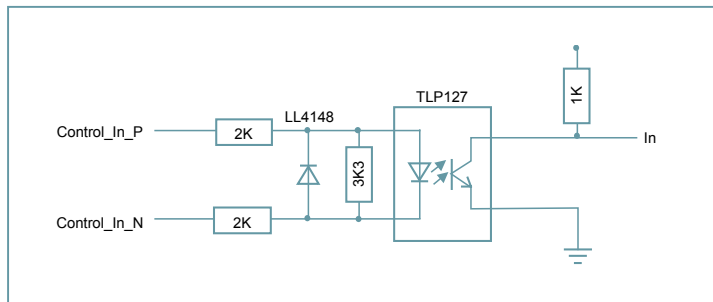
### 3.4.9. DMA Controller

In the last step, image data is transmitted by DMA directly into main memory. This DMA controller consists actually of 20 independent controllers, capable of transferring the video data stream into memory.

**HARDWARE MANUAL PC\_EYE/JPG**

**3.4.10. Opto-Isolated Input Controls**

For control purpose, there are 8 opto-isolated inputs. The inputs do not control any hardware flow, but can be read by software. The diagram below shows the opto-coupler connections:

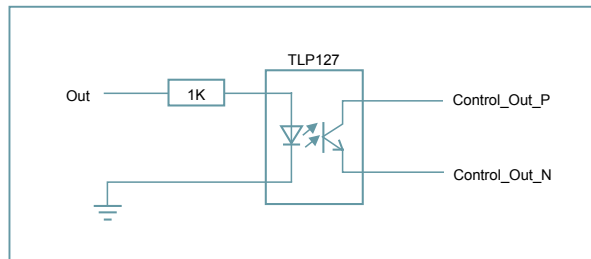


**Figure 9: Optocoupler Input**

An active state is detected, when the input voltage is 3 V or higher. The maximal Voltage is 30 V. For higher voltage, an additional resistor is needed.

**3.4.11. Opto-Isolated Output Controls**

For control purpose, there are 8 opto-isolated outputs. The outputs can be set by writing a register. The diagram below shows the opto-coupler connections:



**Figure 10: Optocoupler Output**

The maximal allowed ON Current is 100 mA. The maximal allowed OFF Voltage is 50 V.

## HARDWARE MANUAL PC\_EYE/JPG

### 3.5. V-PCEY-740 Hardware

#### 3.5.1. Blockdiagram

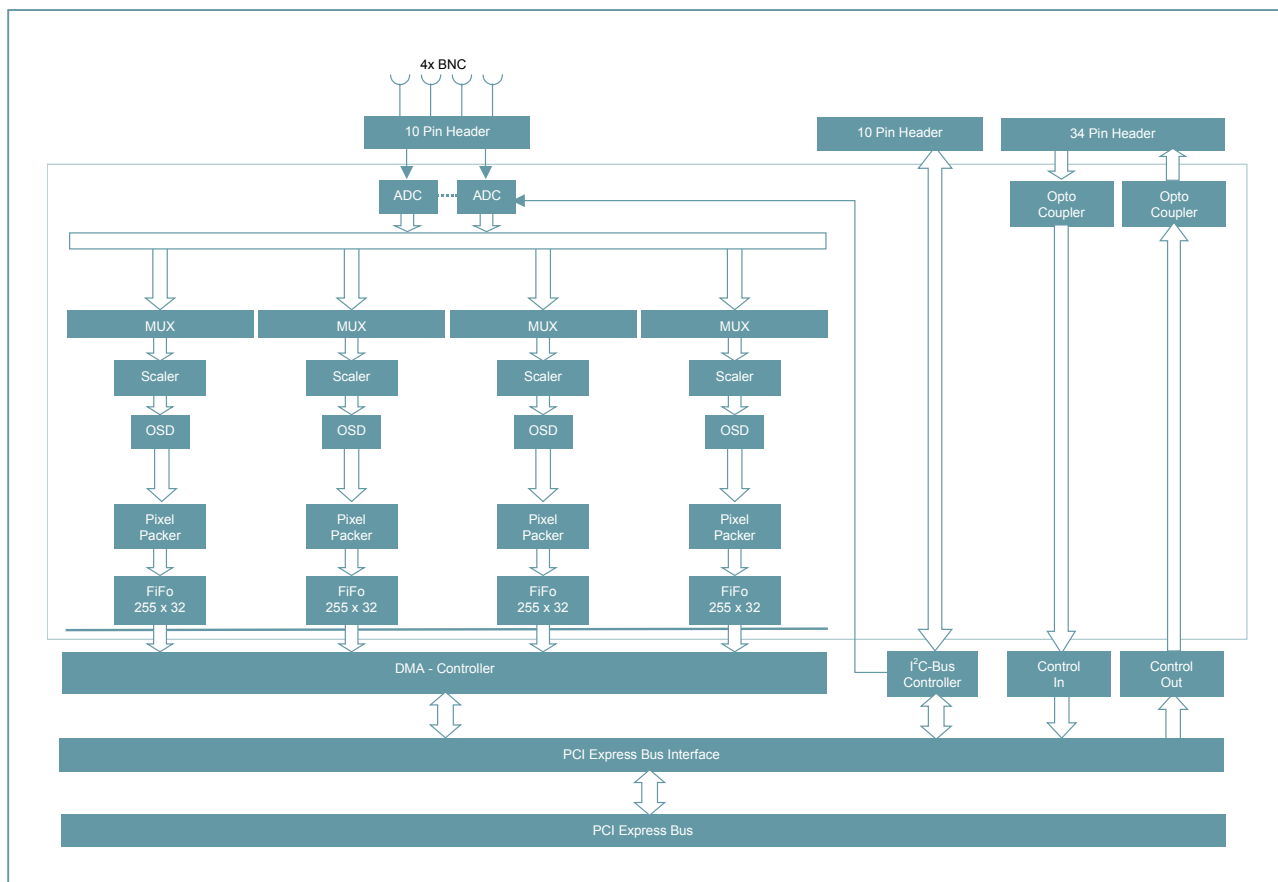


Figure 11: Blockdiagram V-PCEY-740

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## HARDWARE MANUAL PC\_EYE/JPG

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### 3.5.2. Technical Details

The PC\_EYE/JPEG is intended for security applications, where video images from up to four monochrome or color cameras is acquired into a PC's main memory for storage, or the graphics board for display. Images are transferred by up to 4 DMA controllers. An on-board scaling unit can transform the full-resolution images to CIF size for smaller efficient display in split screen applications. Image format can be selected to be luminance / chrominance-separated (YUV) for optimum video detection or to be RGB for display.

### 3.5.3. Camera Signals

The frame grabber board interfaces to standard composite video (CVBS) color cameras, conforming to PAL (NTSC / SECAM) standards. The signals of the cameras are routed to the BNC connectors at the slot bracket.

### 3.5.4. ADC

There are four analog-to-digital converters (ADC) where up to four cameras can be connected to. Each camera has its own ADC (SAA 7113) as well as its own color separator. This makes it possible to switch cameras in the digital domain, minimizing multiplex times: Since the analog input is not switched, there is no PLL settling delay, which can take up to several frame times in other multiplexing schemes. The clock used for acquisition (13.5 MHz) is generated in the ADC chip. It is phase-locked to the horizontal sync.

### 3.5.5. Multiplexer

The digital input multiplexer assigns each of the four (DMA-) channels to one of the four ADC. It is possible to assign on ADC to multiple channels.

### 3.5.6. Scaler

The FPGA-based scaler can be used to reduce video data by line / pixeldropping over original pixels in blocks of 1x1, 2x2, 4x4, or 8x8. By using two DMA channels for storing the same video stream, simultaneous storage of scaled and non-scaled data is possible.

## HARDWARE MANUAL PC\_EYE/JPG

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### 3.5.7. Pixel Packer

To support different cameras and applications, there are several modes of storing pixel data in memory:

**Table 3.5: Pixel Packing Modes**

Mode Name	Description
Mono8	One monochrome image, byte-aligned
Y:U:V	YUV/YCbCr components are stored in 4:4:4, 4:2:2, or 4:1:1 mode
RGB	RGB24 uses 24 bits for each RGB pixel, RGB32 use 32-bit words with one zero-filled byte.

### 3.5.8. FIFO

A FIFO associated with every DMA channel provides buffer space of 1 Kbytes to ensure uninterrupted acquisition even in situations with high PCI bus loads.

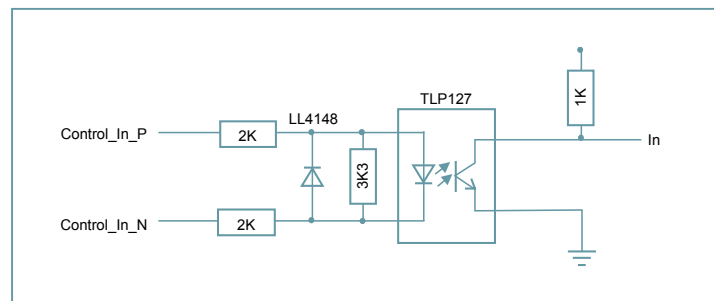
### 3.5.9. DMA Controller

In the last step, image data is transmitted by DMA directly into main memory. This DMA controller consists actually of four independent controllers, capable of transferring the video data stream into memory.

## HARDWARE MANUAL PC\_EYE/JPG

### 3.5.10. Opto-Isolated Input Controls

For control purpose, there are 8 opto-isolated inputs. The inputs do not control any hardware flow, but can be read by software. The diagram below shows the opto-coupler connections:

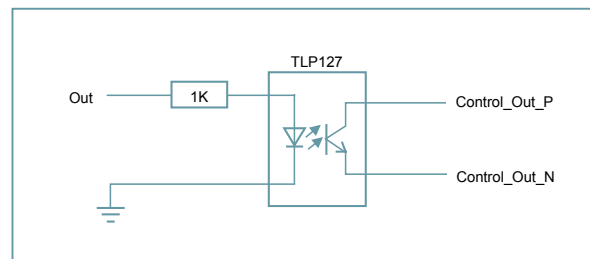


**Figure 12: Optocoupler Input**

An active state is detected, when the input voltage is 3 V or higher. The maximal Voltage is 30 V. For higher voltage, an additional resistor is needed.

### 3.5.11. Opto-Isolated Output Controls

For control purpose, there are 8 opto-isolated outputs. The outputs can be set by writing a register. The diagram below shows the opto-coupler connections:



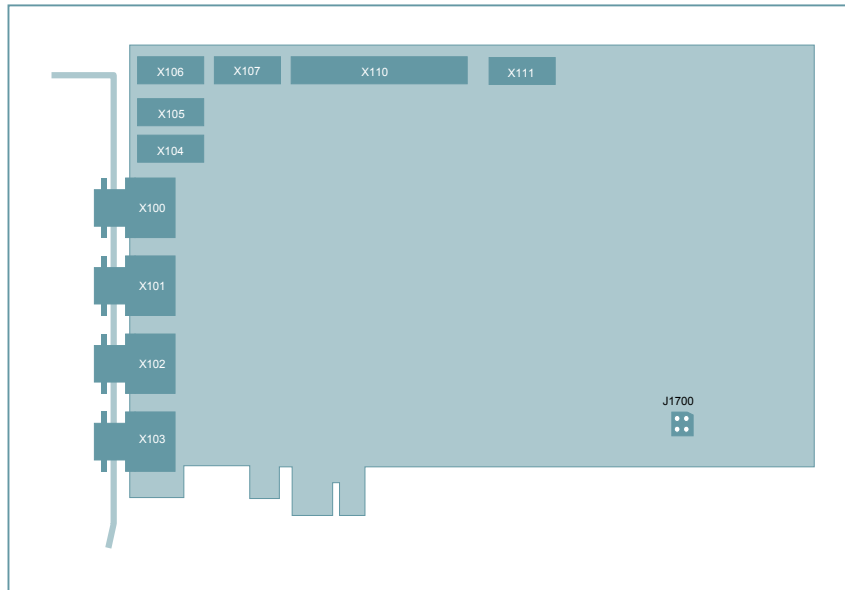
**Figure 13: Optocoupler Output**

The maximal allowed ON Current is 100 mA. The maximal allowed OFF Voltage is 50 V.

**HARDWARE MANUAL PC\_EYE/JPG**

3.6. Switches and Connectors

3.6.1. Connectors and Jumpers Placement



**Figure 14: Connectors and Jumpers Placement**

**Table 3.6: Connectors and Jumpers Content**

Connector	Content
X100	Camera input 0
X101	Camera input 1
X102	Camera input 2
X103	Camera input 3
X104	Camera input 0 to 3
X105	Camera input 4 to 7
X106	Camera input 8 to 11
X107	Camera input 12 to 15
X110	Opto-isolated input and output controls
X111	I2C Bus
J1700	Board-ID select

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### 3.6.2. Connectors and Jumpers Layout

#### 3.6.2.1. Layout BNC Connectors X100 - X103

These connectors contain the camera inputs 0 to 3.

**Table 3.7: Layout BNC Connectors X100 - X103**

Connector	Name	Direction	Description
X100	Video_0	Input	CVBS video input 0
X101	Video_1	Input	CVBS video input 1
X102	Video_2	Input	CVBS video input 2
X103	Video_3	Input	CVBS video input 3

#### 3.6.2.2. Layout 10-Pin Header X104

This connector contains the camera inputs 0 to 3.

**Table 3.8: Layout 10-Pin Header X104**

Pin	Name	Direction	Description
1	GND		Signal ground
2	Video_0	Input	CVBS video input 0
3	GND		Signal ground
4	Video_1	Input	CVBS video input 1
5	GND		Signal ground
6	Video_2	Input	CVBS video input 2
7	GND		Signal ground
8	Video_3	Input	CVBS video input 3
9	GND		Signal ground
10	NC		Not Connected

This connector is optional to use and the signals are identical with the signals on the connectors X100 to X103.

## HARDWARE MANUAL PC\_EYE/JPG

### 3.6.2.3. Layout 10-Pin Header X105

This connector contains the camera inputs 4 to 7.

**Table 3.9: Layout 10-Pin Header X105**

Pin	Name	Direction	Description
1	GND		Signal ground
2	Video_4	Input	CVBS video input 4
3	GND		Signal ground
4	Video_5	Input	CVBS video input 5
5	GND		Signal ground
6	Video_6	Input	CVBS video input 6
7	GND		Signal ground
8	Video_7	Input	CVBS video input 7
9	GND		Signal ground
10	NC		Not Connected

### 3.6.2.4. Layout 10-Pin Header X106

This connector contains the camera inputs 8 to 11.

**Table 3.10: Layout 10-Pin Header X106**

Pin	Name	Direction	Description
1	GND		Signal ground
2	Video_8	Input	CVBS video input 8
3	GND		Signal ground
4	Video_9	Input	CVBS video input 9
5	GND		Signal ground
6	Video_10	Input	CVBS video input 10
7	GND		Signal ground
8	Video_11	Input	CVBS video input 11
9	GND		Signal ground
10	NC		Not Connected

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### 3.6.2.5. Layout 10-Pin Header X107

This connector contains the camera inputs 12 to 15.

**Table 3.11: Layout 10-Pin Header X107**

Pin	Name	Direction	Description
1	GND		Signal ground
2	Video_12	Input	CVBS video input 12
3	GND		Signal ground
4	Video_13	Input	CVBS video input 13
5	GND		Signal ground
6	Video_14	Input	CVBS video input 14
7	GND		Signal ground
8	Video_15	Input	CVBS video input 15
9	GND		Signal ground
10	NC		Not Connected

### 3.6.2.6. Layout 10-Pin Header X110

This connector contains the opto-isolated input and output controls.

**Table 3.12: Layout 34-Pin Header X110**

Pin	Name	Direction	Description
1	Control_In_N_0	Input	Control Negative Input 0
2	Control_In_P_0	Input	Control Positive Input 0
3	Control_In_N_1	Input	Control Negative Input 1
4	Control_In_P_1	Input	Control Positive Input 1
5	Control_In_N_2	Input	Control Negative Input 2
6	Control_In_P_2	Input	Control Positive Input 2
7	Control_In_N_3	Input	Control Negative Input 3
8	Control_In_P_3	Input	Control Positive Input 3
9	Control_In_N_4	Input	Control Negative Input 4
10	Control_In_P_4	Input	Control Positive Input 4
11	Control_In_N_5	Input	Control Negative Input 5

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12	Control_In_P_5	Input	Control Positive Input 5
13	Control_In_N_6	Input	Control Negative Input 6
14	Control_In_P_6	Input	Control Positive Input 6
15	Control_In_N_7	Input	Control Negative Input 7
16	Control_In_P_7	Input	Control Positive Input 7
17	Control_Out_N_0	Output	Control Negative Output 0
18	Control_Out_P_0	Output	Control Positive Output 0
19	Control_Out_N_1	Output	Control Negative Output 1
20	Control_Out_P_1	Output	Control Positive Output 1
21	Control_Out_N_2	Output	Control Negative Output 2
22	Control_Out_P_2	Output	Control Positive Output 2
23	Control_Out_N_3	Output	Control Negative Output 3
24	Control_Out_P_3	Output	Control Positive Output 3
25	Control_Out_N_4	Output	Control Negative Output 4
26	Control_Out_P_4	Output	Control Positive Output 4
27	Control_Out_N_5	Output	Control Negative Output 5
28	Control_Out_P_5	Output	Control Positive Output 5
29	Control_Out_N_6	Output	Control Negative Output 6
30	Control_Out_P_6	Output	Control Positive Output 6
31	Control_Out_N_7	Output	Control Negative Output 7
32	Control_Out_P_7	Output	Control Positive Output 7
33	NC		Not Connected
34	NC		Not Connected

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### 3.6.2.7. Layout 10-Pin Header X111

This connector contains the I2C Bus.





**Table 3.13: Layout 10-Pin Header X111**

Pin	Name	Direction	Description
1	Reserved		Do not connect!
2	Reserved		Do not connect!
3	GND		Signal ground
4	Reserved		Do not connect!
5	SCL	output	Serial clock
6	SDA	I/O	Serial data
7	Reserved		Do not connect!
8	Reserved		Do not connect!
9	Reserved		Do not connect!
10	Reserved		Do not connect!

### 3.6.2.8. Board-ID Jumper J1700

Jumper field J1700 is used to set the board ID. If more than one frame grabber is plugged into the PC, they must have distinct board IDs unequal to zero.

**Table 3.14: Board-ID Jumper Settings**

Jumper Setting	Board-ID
	3
	2
	1
	0

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## HARDWARE MANUAL PC\_EYE/JPG

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### 3.6.3. Status-LED Placement

On the backside, there are 4 LEDs for several status information:

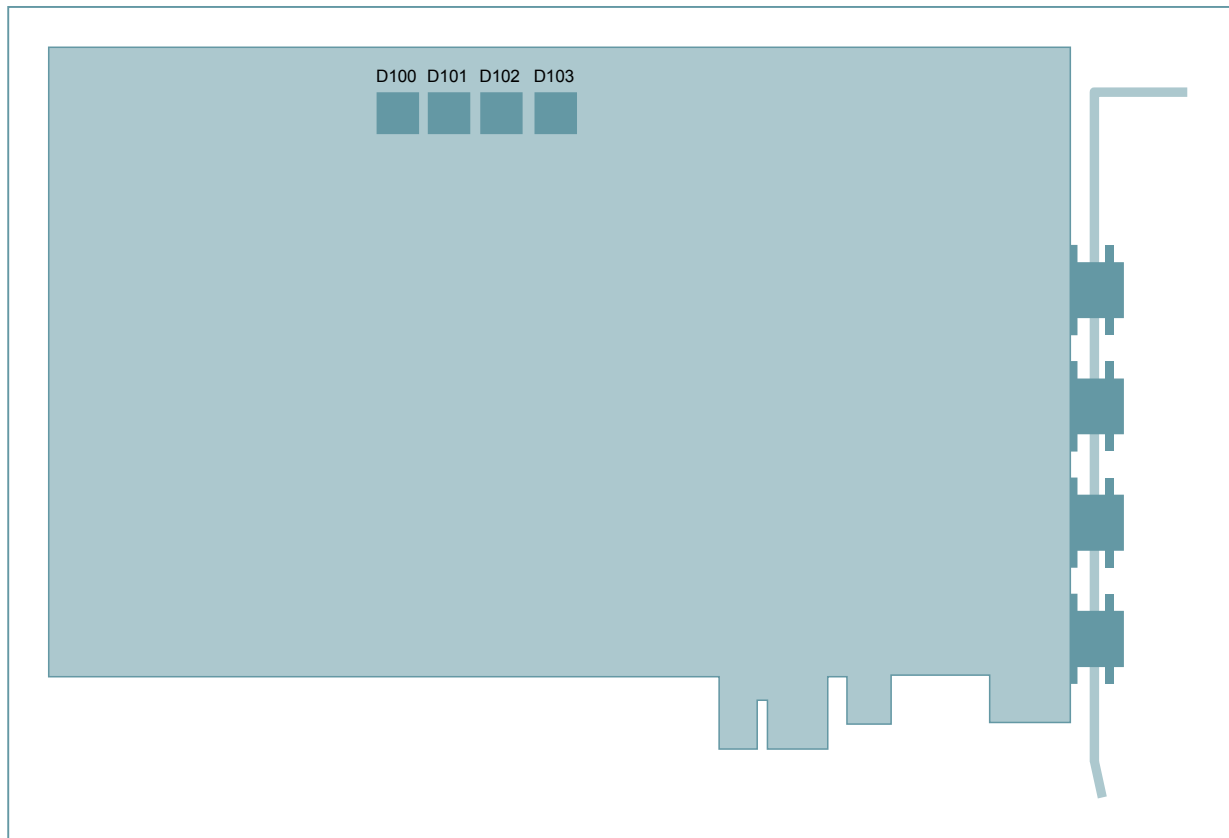


Figure 15: Status-LED Placement

Table 3.15: Frame grabber LED

LED	Description
D100	Board selected - when the frame grabber is initialized, the LED is switched on
D101	Capture - Acquisition in progress, normally flickering
D102	FiFo overrun - The FiFo run full; once set it is shining until the register is reseted
D103	FiFo Write Enable - valid data is written into the FiFo, normally flickering

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### 3.7. Specifications

#### 3.7.1. Electrical Specifications

**Table 3.16: Electrical Specifications**

Description	Min.	Typ.	Max.	Unit
<b>Composite video Inputs</b>				
Video input voltage	0.5	0.7	1.0	Vpp
Sync input voltage	0.2	0.3	0.4	Vpp
Offset input voltage	-2		+2	V
<b>Optical Isolated Inputs</b>				
Logical low	-30		2	V
Logical high	3		30	V
<b>Optical Isolated Outputs</b>				
OFF voltage	3		30	V
ON current			100	mA
Saturation voltage	0.5		0.75	V
<b>Power Requirements</b>				
Power Supply +12 V		0.45	0.5	A
Power Supply +3.3V		1.7	1.9	A

#### 3.7.2. Environmental Conditions

Storage Temperature:	-20 °C - 70 °C
Operating Temperature:	0 °C - 55 °C (0,1 m/s forced air cooling)
Maximum Operating Humidity:	85 % relative

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NOTES